503.37770X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: M. OGINO, et al.

Serial No.: 09/429,297

Filed: October 28, 1999

For: SEMICONDUCTOR DEVICE, SEMICONDUCTOR WAFER, SEMICONDUCTOR MODULE, AND A METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Group: 2822

Examiner: James M. Mitchell

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

December 10, 2002

Sir:

In response to the Office Action mailed July 10, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims presently in the application as follows:

2. (Twice Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip, and

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of the semiconductor device on a same plane.

3. (Twice Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

via-holes provided between the electrodes on said semiconductor chip and said circuit layer,

conductive portions for connecting electrically said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of the semiconductor device on a same plane.

9. (Twice Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said circuit layer and said electrodes on said semiconductor chip,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed to outside of said semiconductor device on a same plane.

Please add the following new claims to the application:

--27. A semiconductor device as claimed in any one of claims 2, 3, 9, 10, 11 and 17, wherein the porous stress relaxing layer has a breathing property.

28. A semiconductor device as claimed in any one of claims 2, 3, 9, 10, 11 and 17, wherein said porous stress relaxing layer is made of a material selected from the group consisting of polycarbonate, polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide and polyimide.--

REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, each of claims 2, 3 and 9 has been amended to recite that respective side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film are exposed "to" outside of the semiconductor device on a same plane. Note previously considered claims 10, 11 and 17. See also, for example, Fig. 1(i), showing the "semiconductor device" having the stress relaxing layer (see reference character 3 in Fig. 1(b)), the semiconductor chip (note for example, reference character 6 of Fig. 1(c), showing the wafer) and the organic protecting film (note, for example, reference character 7 in Fig. 1(c), showing the wafer protecting film), Fig. 1(i) showing side planes of the recited structures exposed to outside of the semiconductor device on a same plane.

In addition, Applicants are adding new claims 27 and 28 to the application. Claim 27, dependent on any one of claims 2, 3, 9, 10, 11 and 17, recites that the porous stress relaxing layer has a breathing property. Note, for example the paragraph bridging pages 8 and 9 of Applicants' Substitute Specification, submitted with the Preliminary Amendment filed March 31, 2000. As for what is meant by "breathing property", note the definition thereof at page 9, lines 18-21 of this Substitute Specification. Claim 28, also dependent on any one of claims 2, 3, 9, 10, 11 and 17, defines material of the porous stress relaxing layer, consistent with the description at page 10, lines 14-19, of this Substitute Specification. As can be appreciated, aromatic polymers such as aromatic polyester, aromatic polyamide and aromatic polyimide are respectivelyincluded within the recited polyester, polyamide and polyimide.

Applicants respectfully traverse the rejection of their claims under the second paragraph of 35 USC 112, as being indefinite, particularly insofar as this rejection is applicable to claims as presently amended. Thus, note that claims 2, 3 and 9 have been amended to recite that the respective side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film are exposed to outside of the semiconductor device on a same plane. For example, and as shown in Applicants' drawing figures (for example, note Fig. 1(i), Fig. 3(h) and Fig. 4(b), as well as other figures), the obtained semiconductor device is in a condition that the stress relaxing layer, the semiconductor chip and the protecting film are exposed to outside of the semiconductor device at the cutting plane (corresponding to the side plane of the semiconductor device) as shown in Fig. 4(b). That is, for example, in cutting the wafer to a size of each chip unit, as shown, for example, in Fig. 1(i), side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film are exposed to outside of the semiconductor device on a same plane. Clearly, the present claims define structure which sufficiently defines metes and bounds of the present invention, such that one of ordinary skill in the art would know whether any particular semiconductor device fell within or outside the scope of the present claims. Under the present circumstances, the second paragraph of 35 USC 112 requires nothing more. See In re Moore, 169 USPQ 236 (CCPA 1971).

As will be discussed further infra , according to the present invention the semiconductor device produced has the porous stress relaxing layer exposed to the outside (for example, exposed to the atmosphere), which makes it possible to release a high vapor pressure generated at a re-flow operation and to obtain a highly reliable semiconductor device.

The contention by the Examiner in Item 4 on page 2 of the Office Action mailed July 10, 2002, that it is ambiguous as to how side planes of the device, which are formed after being "singulated", are exposed outside of the device which they comprise, is noted. It must be emphasized that the side planes of the device are formed, e.g., by the cutting, the side planes being, e.g., the cut plane such that the side planes are exposed to the outside of the semiconductor device. It is respectfully submitted that, contrary to the contention by the Examiner, the claimed structure is not ambiguous, but rather the claims sufficiently define the present so as to satisfy the requirements of the second paragraph of 35 USC 112.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references as applied by the Examiner in rejecting claims in the Office Action mailed July 10, 2002, that is, the teachings of the U.S. Patents to Kim, et al., No. 6,004,867, to Ball, et al., No. 6,351,022, and to Chang, et al., No. 6,353,182, and European Patent Application No. 504,669 (Fukutake), under the provisions of 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a semiconductor device, or such a semiconductor wafer, or such module of a plurality of semiconductor devices, as in the present claims, having the porous stress relaxing layer provided on a plane of a semiconductor chip on which the circuits and electrodes of the chip are formed, with a circuit layer provided on the stress relaxing layer, and with an organic protecting film provided on the plane of the chip opposite to the stress relaxing layer, and wherein side planes of the stress relaxing layer are exposed to outside of the semiconductor device (note claims 2, 3, 9, 10, 11 and 17); or, more

particularly, wherein respective side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film are exposed to outside of the semiconductor device on a same plane (see claims 2, 3 and 9).

Furthermore, it is respectfully submitted that these references would have neither disclosed nor would have suggested such a semiconductor device as in the present claims, including the recited structure having the porous stress relaxing layer, and wherein this porous stress relaxing layer has a breathing property (see claim 27); and/or has a greater porosity than that of the organic protecting film (see claim 25); and/or wherein the porous stress relaxing layer is made of a material selected from the specific group of materials listed in claim 28, in particular, is made of a porous polytetrafluoroethylene (see claims 5 and 13).

In addition, it is respectfully submitted that these references would have neither taught nor would have suggested such device, or such wafer, as in the present claims, wherein the side planes of the recited structures, which are exposed to outside of the semiconductor device, form a peripheral edge of the respective structures. See, for example, claims 21 and 22.

Moreover, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a semiconductor device or wafer as in the present claims, including the stress relaxing layer, chip and organic protecting film as discussed previously, and wherein the organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of the stress relaxing layer (note, e.g., claim 4), and/or wherein the stress relaxing layer is adhered to the semiconductor chip by an adhesion layer, with a linear expansion coefficient of the organic protecting film being substantially

equivalent to the linear expansion coefficient of the adhesion layer (see claim 23; note also claim 24).

Furthermore, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a semiconductor device as in the present claims, and including additional aspects of the present invention as in the remaining, dependent claims, including (but not limited to) wherein the organic protecting film is colored black (see claim 26).

The present invention as claimed in the above-identified application is directed to a semiconductor device having a chip size package (CSP) of the type used for a high density mounting module, a wafer having a chip for such semiconductor device, and a multichip module utilizing such semiconductor device.

A chip size package manufactured by steps of forming bumps on a wafer, connecting the wafer with a substrate, sealing the interval between the substrate and wafer with a resin, forming external electrodes, and cutting the wafer into respective devices, has a problem of warping of the wafer and semiconductor device due to curing shrinkage, because the resin layer was formed on only one side of the wafer. Additionally, many of the CSPs have an exposed plane, which is opposite to the plane whereon the circuits are formed on the chip. Therefore, there is a problem in that failures, such as cracks, are generated at the edge of the chip, and damage to the rear plane occur due to the package falling (e.g., being dropped) during transportation and handling, such as when the package is picked up during a mounting operation.

An additional problem arising in connection with CSPs, using a resin substrate, is that water absorbed in the package expands, e.g., at re-flow, and

failures, such as bubble formation and peeling, occur.

Against this background, Applicants provide structure which avoids the foregoing problems, the structure in particular avoiding problems due to moisture and breakage, as well as avoiding warping. Applicants have found that by utilizing a porous stress relaxing layer which is exposed to the outside of the semiconductor device (e.g., at a side plane of the device), this stress relaxing layer being used together with an organic protecting film provided on an opposite side of the chip to that provided with the stress relaxing layer, objectives according to the present invention are achieved. Specifically, by utilizing a porous stress relaxing layer, with side planes thereof exposed to outside of the semiconductor device, the porous stress relaxing layer having, e.g., a breathing property as defined in Applicants' original disclosure, moisture absorbed can be released outside of the package through the porous stress relaxing layer, thereby avoiding possible cracking and peeling due to, e.g., expansion of the moisture at mounting re-flow.

In addition, by utilizing the porous stress relaxing layer and organic protecting film on opposite sides of the chip, with the side planes and the various structures exposed to outside of the semiconductor device on a same plane, damage due to expanding moisture upon re-flow can be avoided, as discussed previously; and, moreover, warping of the device, or cracking where the device is dropped, can be avoided. In this regard, through exposure of the various structures outside of the semiconductor device on the same plane, as in various of the present claims, damage to edge portions of the chips and cracks are scarcely generated.

Furthermore, according to the present invention having the exposed side planes, the wafer, stress relaxing layer and organic protecting film, as well as, e.g.,

the circuit layer, can be cut simultaneously along a same plane to form respective units, simplifying the processing. In addition, any difference in package area relative to chip area can be reduced, because the wafer, stress relaxing layer and circuit layer can be cut simultaneously along a same plane to form respective units.

As for advantages achieved according to the present invention, note the description in Applicants' Substitute Specification on page 47, line 9 to page 48, line 17. That is, the present invention achieves various advantages such as avoiding failure during mounting re-flow; at the least, reducing the amount of warp of the package; avoiding damage and cracks when dropping the device; and substantially no difference in package area relative to the chip area, because, for example, the wafer stress relaxing layer, chip and circuit layer can be cut simultaneously along a same plane.

With respect to the present invention, attention is respectfully directed to Table 1 on pages 21-23 of Applicants' Substitute Specification. This Table 1 reports results in connection with various Embodiments of the present invention and Comparative examples with respect to the present invention, described the beginning from page 16 of Applicants' Substitute Specification. It is respectfully submitted that this evidence in Applicants' Specification shows unexpectedly better results achieved according to the present invention, with respect to decreased warp of the wafer and of the package; decreased failure generation rate after 1000 cycles; decreased failure generation rate in a re-flow test; reduced failure generation rate in a dropping test; and decreased ratio of package area to chip area, as compared with various conditional structures, and further supports unobviousness of the presently claimed subject matter. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984).

Kim discloses a chip-size package and method of manufacture thereof. The chip-size package includes a semiconductor chip having a plurality of input/output pads on an active surface thereof, and a passivation layer covering the active surface such that the input/output pads are exposed. The chip-size package further includes a plurality of electrically conductive traces and corresponding terminal pads in a substrate having a bottom surface and a top surface. A bottom portion of each of the traces is exposed at the bottom surface, and the bottom surface of the substrate is attached to the passivation layer so that the bottom portion of each of the traces is mechanically and electrically bonded to a respective one of the input/output pads. A plurality of metallic bumps are formed on a top portion of respective ones of the terminal pads, so that each of the bumps is electrically connected with a respective one of the input/output pads of the semiconductor chip through the respective one of the traces and the terminal pads. See from column 1, line 53 to column 2, line 5. Note also Figs. 1 and 2, and the corresponding description at column 2, lines 62-67 and column 3, lines 13-15. Note also Figs. 4 and 5(A) and the corresponding description in connection therewith at column 5, lines 16-26; this description includes a passivation layer 314 covering the active surface so that the input/output pads 312 are exposed.

It is respectfully submitted that this disclosure of Kim, et al. would have neither taught nor would have suggested various aspects of the present invention, including, inter alia, the porous stress relaxing layer, particularly with side planes thereof exposed to the outside of the semiconductor device, or other aspects in the present invention as discussed in the foregoing.

The contention by the Examiner that Kim, et al. discloses "an inherent porous,

stress release, Silicon dioxide layer (314; pores created by space within layer for pad)" is respectfully traversed. Layer 314 of Kim, et al. is passivation layer, which effectively acts as a protection layer of the active surface. Such disclosure of a passivation layer would have taught away from a porous layer, as in the present claims.

Moreover, Applicants respective traverse any conclusion by the Examiner that the passivation layer of Kim, et al. is "inherently" a stress release (appropriately, in the present claims, relaxing) layer. The Examiner has provided no evidence or reasoning for such conclusion of the passivation layer being a stress release or relaxing layer. Absent such evidence or reasoning, clearly the rejection is improper. See In re McKellin, 188 USPQ 428 (CCPA 1976).

It is respectfully submitted that the teachings of Ball, et al., would not have rectified the deficiencies of Kim, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Ball, et al. discloses a system for processing a planar structure, such as a semiconductor wafer. According to this patent, semiconductor wafers are segmented prior to being ground, and the segmented wafer portions are supported on a wafer holding table for grinding. By segmenting the wafers before reducing their thickness by grinding, the problem of wafers cracking and breaking during dicing is reduced. See column 2, lines 4-9. This patent discloses that, in operation, protective material, such as polyimide tape or polyamide coatings, is applied to the front and back surfaces of the wafer. The wafer is then segmented into quarter-sized wafer portions; and then the back protective coating is removed from the wafer portions, and the wafer portions are moved to a grinding apparatus by suitable pick

and place equipment. After the grinding process is completed, the wafer portions are moved individually by suitable pick and place equipment to another station for removal of the front protective coatings, for dicing into individual chips, and for further processing. See column 3, lines 25-34.

It is emphasized that in Ball, et al., both the front and rear protective coatings are removed, for example, prior to dicing into individual chips. In any event, clearly neither of the front nor rear protective coatings are on the individual semiconductor chips after the dicing. It is respectfully submitted that the teachings of Ball, et al. would have neither disclosed nor would have suggested, and in fact would have taught away from, the presently claimed subject matter, including the semiconductor device having the recited organic protecting film, in particular, such organic protecting film providing on the plane opposite to the stress relaxing layer of the semiconductor chip.

Furthermore, it is respectfully submitted that the teachings of Ball, et al. and of Kim, et al., in combination, would have neither disclosed nor would have suggested the porous stress relaxing layer provided on a plane of the semiconductor chip whereon circuits and electrodes are formed, much less the exposed side planes of the various components, or the circuit layer provided on the stress relaxing layer, and advantages thereof as in the present invention.

Chang, et al. discloses packaging semiconductor devices with laminar substrates using the flip-chip packaging technique, this patent disclosing a selection of techniques that improve reliability of a flip-chip plastic ball grid array assembly. See column 2, lines 60-62. In one embodiment, this patent discloses matching the z-direction coefficient of thermal expansion (CTE) of the IC solder joint with the z-

direction CTE of the encapsulant. Note column 3, lines 32-45. See also column 2, lines 48-57; column 2, line 64 to column 3, line 4; and column 4, line 8-12, 48, 49 and 54-57.

It is respectfully submitted that Chang, et al. is directed to particular problems arising in connection with a flip-chip plastic ball grid array assembly. It is respectfully submitted that one of ordinary skill in the art concerned with in Kim, et al., i.e., chip-size packages, would not have looked to the teachings of Chang, et al. That is, in view of the different technologies involved with Kim, et al., on the one hand, and in Chang, et al., on the other, and different problems addressed by each, one of ordinary skill in the art concerned with in Kim, et al. would not have looked to Chang, et al. (these references are directed to non-analogous arts).

In addition, it is respectfully submitted that there would have been no proper motivation for combining the teachings of Kim, et al. and Chang, et al., as applied by the Examiner. In this regard, note that Chang, et al., in one embodiment, matches z-direction CTEs of the IC solder joint and the encapsulant. It is respectfully submitted that such disclosure would have neither taught nor would have suggested, either alone or in combination with the teachings of Kim, et al., and Ball, et al., the relative linear expansion coefficients of the organic protecting film and stress relaxing layer; or relative linear expansion coefficients of the organic protecting film and the adhesion layer, as in the present claims.

In addition, it is respectfully submitted that the combined teachings of Kim, et al., Ball, et al. and Chang, et al. would have neither disclosed nor would have suggested the stress relaxing layer, much less porous stress relaxing layer, and side planes of specified structure being exposed to outside of the semiconductor device,

or circuit layer provided on the stress relaxing layer, and advantages thereof as in the present invention.

Fukutake discloses a semiconductor device that carries an integrated-circuit chip or another semiconductor element on a substrate, and having a porous polytetrafluoroethylene layer positioned between the semiconductor element and the substrate. This patent discloses that because of the presence of this layer, the stress which is generated inside the integrated-circuit chip is alleviated, thereby increasing the reliability of semiconductor devices. See column 2, lines 22-33; note also column 2, lines 11-21; column 3, lines 33-36; and column 4, lines 39-45.

It is emphasized that Fukutake discloses an encapsulating package. It is respectfully submitted that one of or ordinary skill in the art concerned with in Kim, et al., directed to chip-size packages, would not have looked to the teachings of Fukutake. Moreover, again emphasizing that Kim, et al. has passivation layer 314, such passivation layer generally being provided on a semiconductor chip in order to shield and protect elements formed on the surface of the chip, one of ordinary skill in the art would not have looked to the porous PTFE layer of Fukutake in connection with this passivation layer.

In any event, even assuming, arguendo, that the teachings of Fukutake were properly combinable with the teachings of the other references as applied by the Examiner, such combined teachings would have neither disclosed nor would have suggested the presently claimed structure, including the porous stress relaxing layer having side planes thereof exposed to outside of the semiconductor device, much less wherein side planes of the stress relaxing layer, the chip and the organic protecting film are exposed to outside of the semiconductor device on a same plane,

and, moreover, wherein a circuit layer is provided on the stress relaxing layer, as in the present claims.

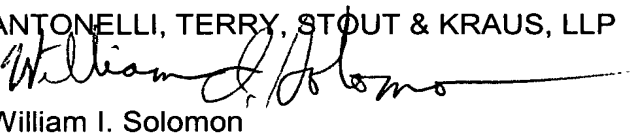
In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application and being considered on the merits therein are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The changes are shown on the attached pages, the first page of which is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 503.37770X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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